

Figure 1

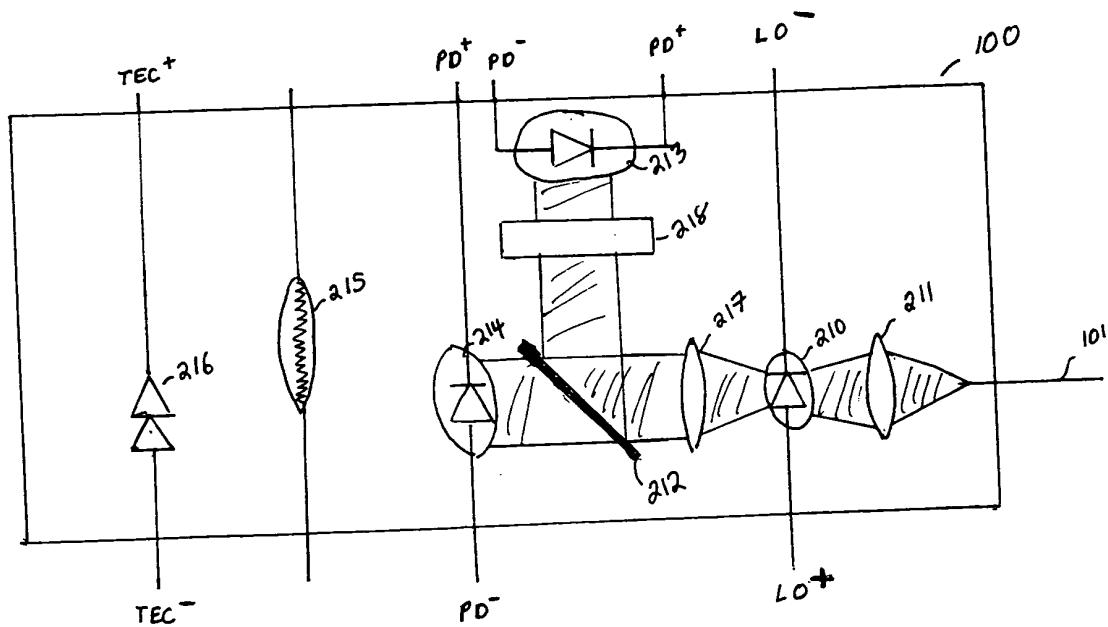


Figure 2

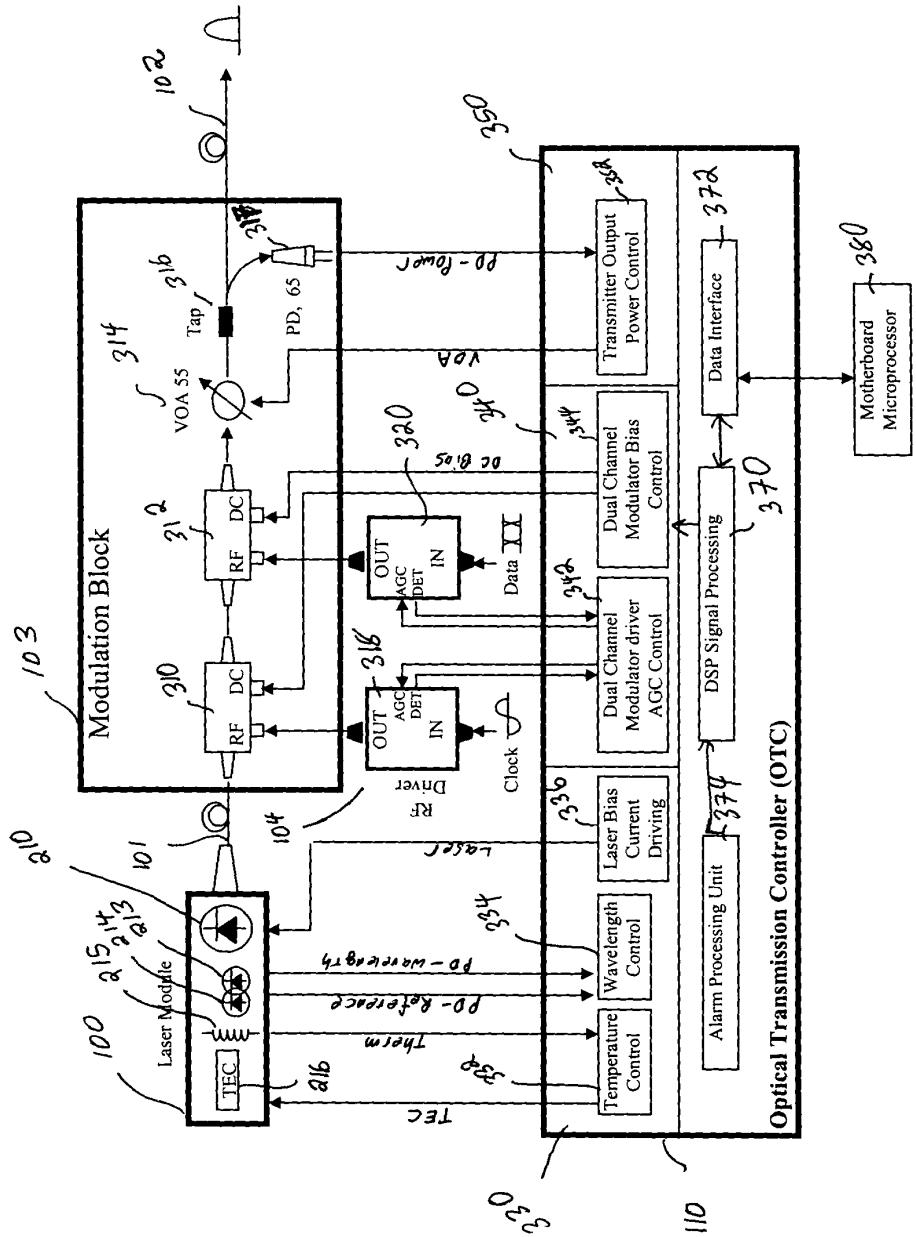


Figure 3

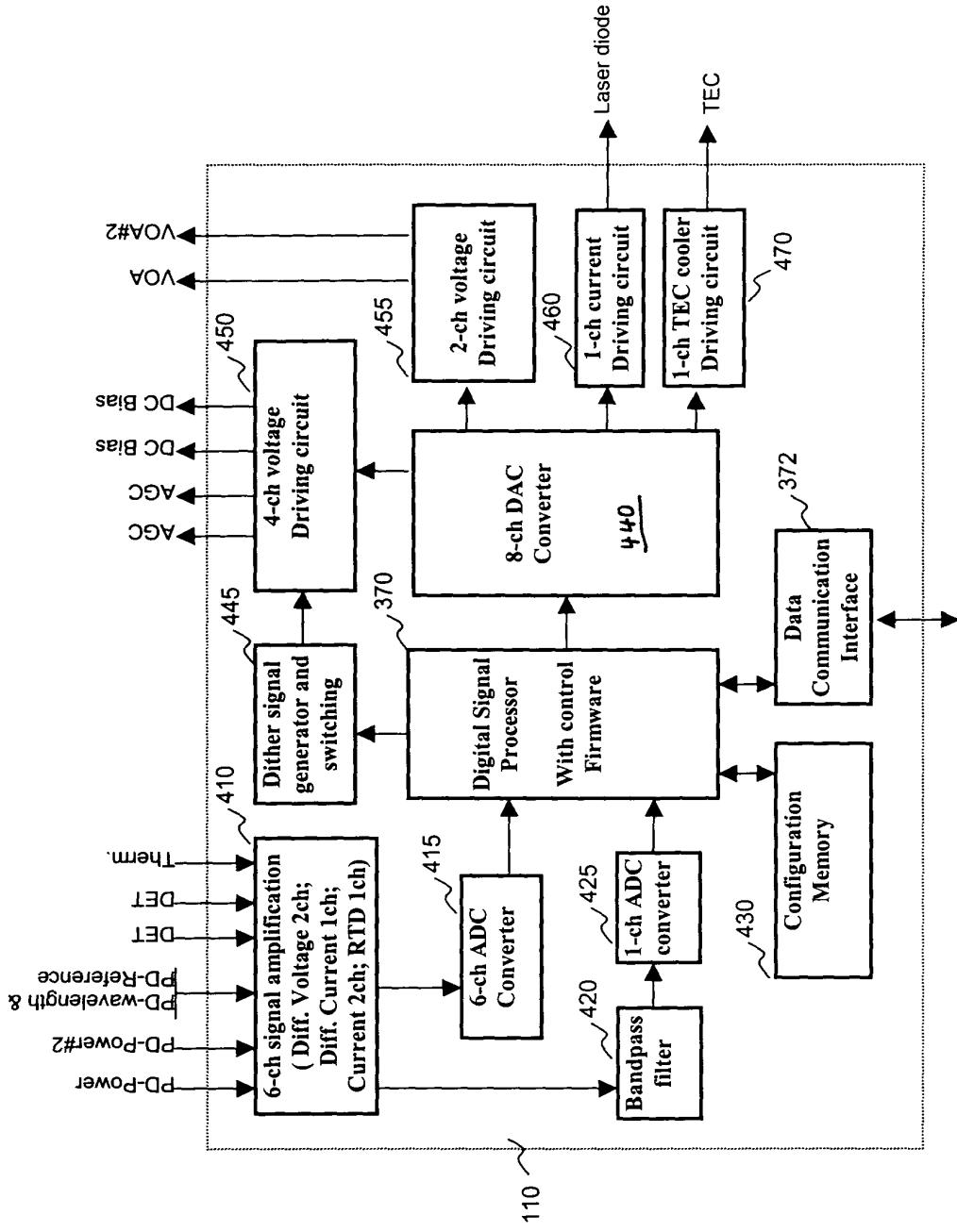


Figure 4

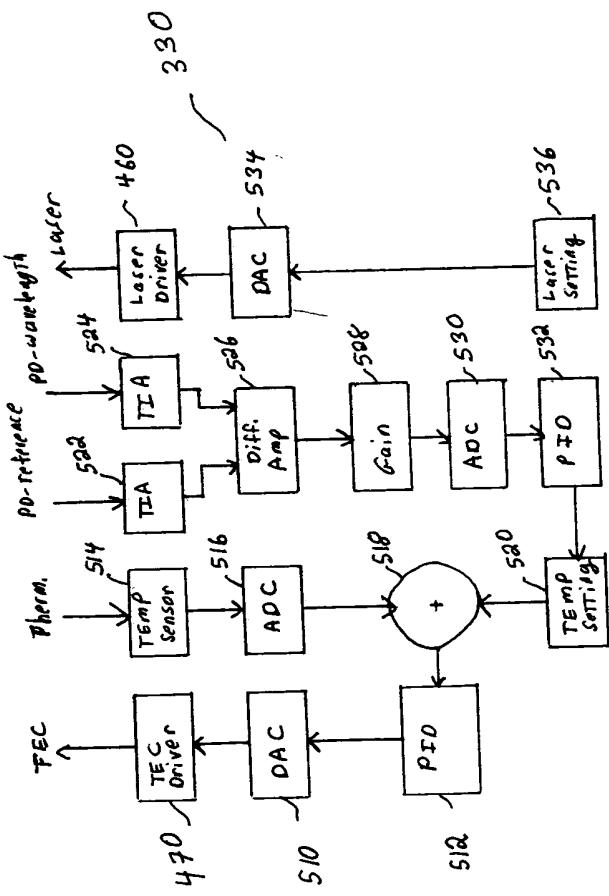


Figure 5 A

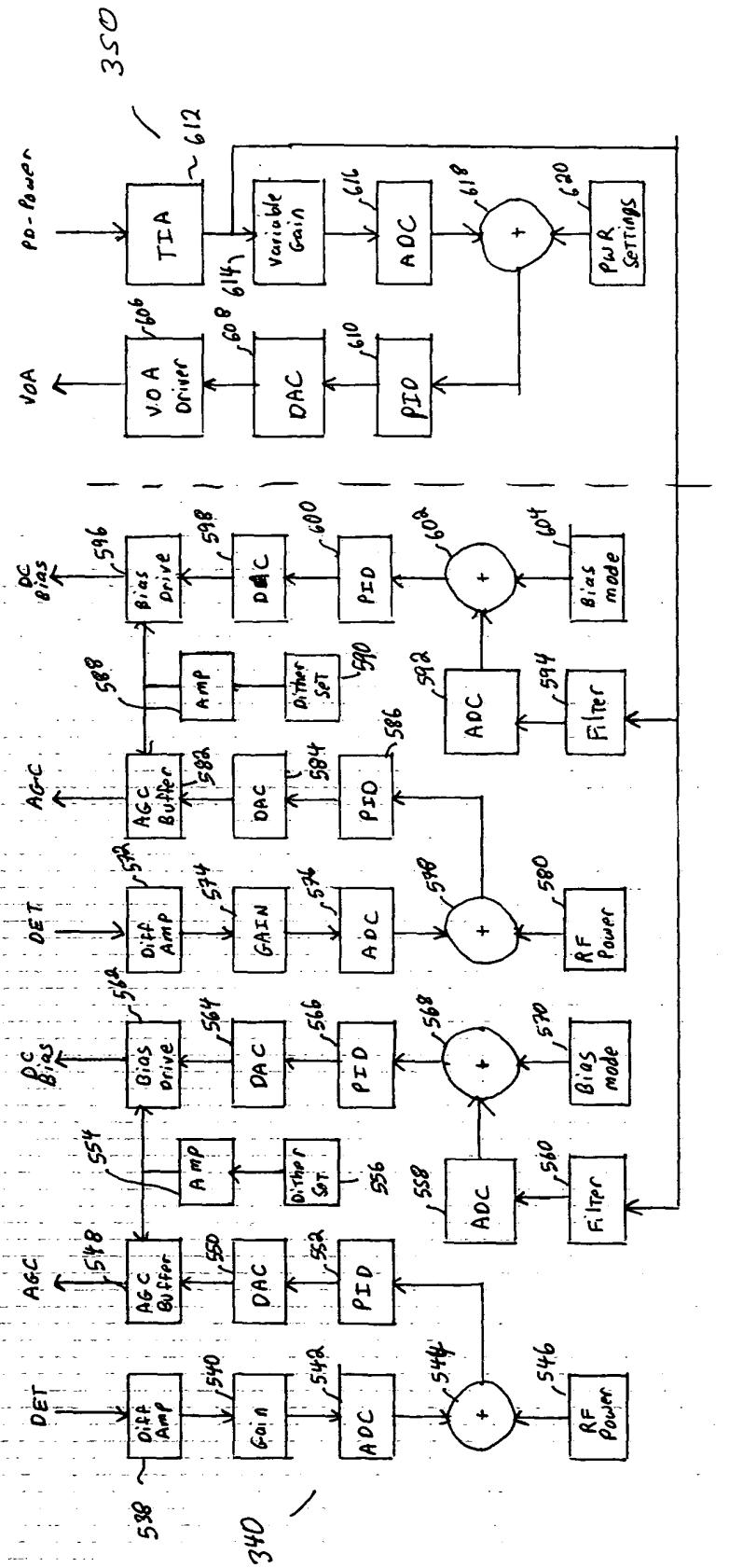


Figure 5B

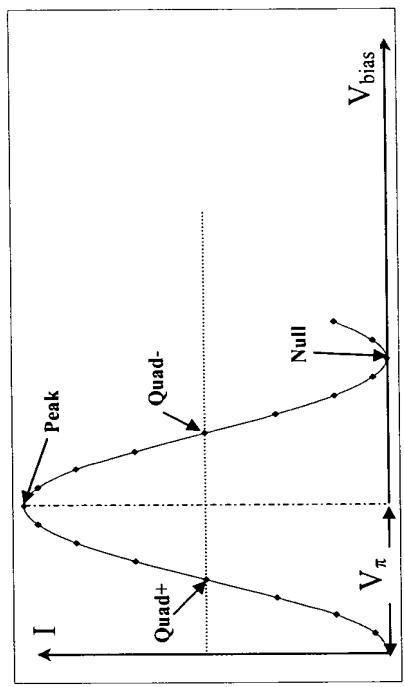


Figure 6

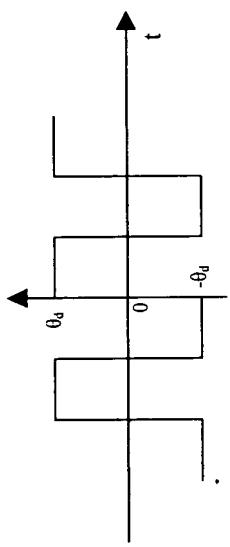


Figure 7A

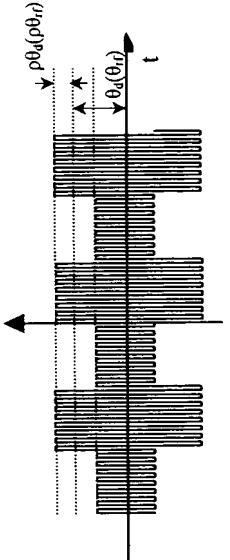


Figure 7B

Bias Mode	RF Driving	Error signal amplitude normalized to $P_m$
Gated square dither to DC port for Quad+ control	Sinusoidal	$-2\pi * \sin \theta_{dc} * \sin \theta_d * \sin (\rho \theta_d) * \text{BesselJ}(0, \theta_{rf})$
Square dither to modulator driver for Quad+ control	Square Digital	$-2\pi * \sin \theta_{dc} * \sin \theta_d * \sin (\rho \theta_d) * \cos \theta_{rf}$
Square dither to DC port for Peak control	Sinusoidal	$-\rho/\pi * \sin \theta_{dc} * [1 - \text{BesselJ}(0, 2\theta_{rf})]$
Square dither to DC port for Peak control	Square Digital	$-2\pi * \sin \theta_{dc} * \sin \theta_{rf} * \sin (\rho \theta_{rf})$
Square dither to DC port for Peak control	Sinusoidal	$-2\pi * \sin \theta_{dc} * \sin \theta_d * \text{BesselJ}(0, \theta_{rf})$
Square dither to DC port for Peak control	Square Digital	$-2\pi * \sin \theta_{dc} * \sin \theta_d * \cos \theta_{rf}$

Figure 7C

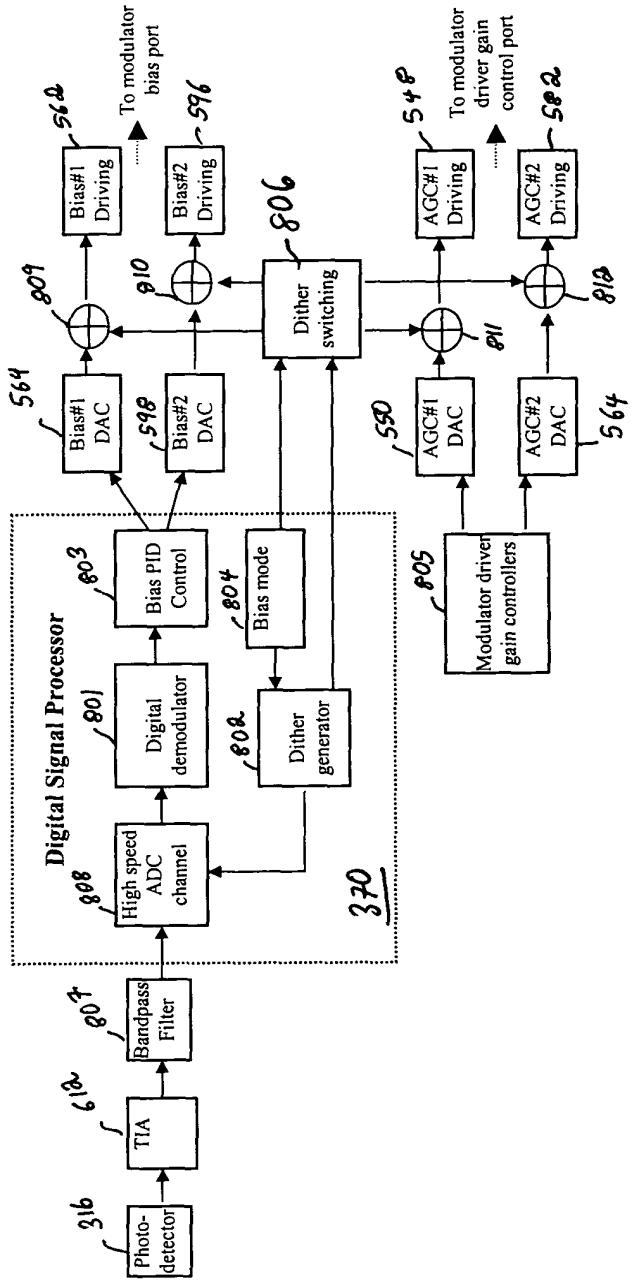


Figure 8